Amendments to the Drawings

Please approve amendment to the drawings by labeling Figs. 1 – 4 as "Prior Art".

REMARKS

Status of Claims

Claims 1 – 30 were original in the application. Claims 2 – 4, 7, 10, 16, 24, 28, and 29 have been cancelled. Claims 1, 5, 6, 8, 9, 11, 12, 17, 25, and 26 have been currently amended. Claims 1, 5, 6, 8, 9, 11, 15, 17 – 23, 25 – 27 and 30 are submitted for examination on the merits.

Preliminary Statement

The claims define at least two novel features. One is a diode used as the capacitive element to reduce the loading capacitance of a Darlington pair, thereby minimizing the signal distortion in an ESD integrated chip. The other is the series of a diode and a resistor used as the trigger control element to reduce the leakage current at low to medium RF power level for better linearity and efficiency. They both can be incorporated into the ESD protection circuit design in order to meet the RF IC applications. In addition, the claimed circuit has additional advantages such as providing the RF mismatching and protection at the input/output signal terminals.

Rejection Pursuant to 35 USC 102

1. Claims 1 - 3, 7, 12 - 14, 21, 25 - 26 and 28 were rejected as being anticipated by McClure et al., Patent No. 5,774,318.

With respect to claim 1, the Examiner contended that McClure teaches an electrostatic discharge protection circuit [Fig. 2] coupled to ground [Fig. 2, 104]

comprising: an input [Fig. 2, Vcc 102]; a diode string [Fig. 2, 100] coupled to the input; a transistor switch [Fig. 2, 03, 106] having its gate coupled to the diode string, the transistor switch coupling the input to ground in parallel to the diode string; and a reverse diode [Fig. 2, 116] coupling ground to the input as disclosed in Col. 3, lines 19-25 and lines 44-48.

McClure's circuit is for protection of positive and negative voltage power supply terminals as stated in col. 1, lines 6 - 8. By its title, claims and nearly every paragraph of its disclosure McClure is exclusively directed to power supply terminals. In contrast, the claimed circuit can be used for **both** protection of input/output signal paths of a RF integrated circuit as shown in Fig. 5, as well as the voltage power supply terminals. The fact that protection of input/output signal paths of a RF integrated circuit is provided makes the claimed invention a completely different application. The difference is very significant. ESD protection at signal path is more difficult than protection at the voltage power supply terminal.

Extra loading capacitance at the signal path can distort signal, which typically cannot be tolerated at an input/output signal terminal. Because the claimed circuit is used at input/output signal paths, a diode 24, is connected in series with the switch 16 in Fig. 5, so that its loading capacitance is reduced to minimize input/output signal distortion. For voltage power supply terminal protection as used in McClure, loading capacitance is not an issue since there is no input/output signal involved. Should McClure be used in an input/output signal path of a RF integrated circuit, as in our claim, it would be inoperable due to the large loading capacitance and that cause signal distortion.

With respect to claim 12, the Examiner contends that McClure teaches a method for providing electrostatic discharge protection comprising sinking a first type of ESD event to ground [Fig. 1, GND 104] from an input [Fig. 1, Vcc, 102] through a diode string [Fig. 1, 100] coupled to the input by triggering a transistor switch [Fig. 1, 03, 106] having its gate coupled to the diode string, the transistor switch coupling the input to ground in parallel to the diode string; and sinking a second type of ESD event through a reverse diode [Fig. 1, 116] coupling ground to the input [Col. 3, lines 19-25, lines 38-41, lines 44-48, Col. 5, lines 7-16, Col. 6, lines 18-21].

The distinctions made with respect to claim 1 are herein reincorporated with respect to claim 12. McClure's methodology exclusively protects voltage power supply terminals as stated in its title, claims and nearly every paragraph of its disclosure. In contrast, the claimed circuit is directed to the protection of input/output signal paths of a RF integrated circuit as shown in Fig. 5. The difference is very significant.

Extra loading capacitance at the signal path can distort signal, which typically cannot be tolerated at an input/output signal terminal. Claim 12 as amended practices the step of coupling the input/output signal terminal to ground during ESD protection by means of a capacitive element in series with the transistor switch to reduce the capacitance contributed from the transistor switch. Should McClure's method be used in an input/output signal path of a RF integrated circuit, as in the claimed methodology, it would be inoperable due to the large loading capacitance and signal distortion.

Claim 13 serves to further define the steps of claim 12 and is allowable therewith.

With respect to claim 21, the Examiner contends that McClure teaches that the diode string [Fig. 2, 100] is comprised of a plurality of BC junction diodes [Fig. 3, 115].

The Applicants respectfully disagree with the Examiner's contention. There is no disclosure whatsoever in McClure that base-collector junction diodes are used for any purpose, let alone that claimed in claim 21. There is no characterization of diodes 115 provided in McClure.

With respect to claim 25, the Examiner contends that McClure teaches an ESD protected bonding pad comprising a first pad [Fig. 2, Vcc, 102]; a diode string [Fig. 2, 100] coupled to the first pad; a transistor switch [Fig. 2, 03, 103] having its gate coupled to the diode string, the transistor switch coupling the first pad to ground in parallel to the diode string; and a reverse diode [Fig. 2, 116] coupling ground to the first pad as disclosed in Col. 3, lines 19-25 and lines 44-48.

The remarks made with respect to claim 1 are reincorporated herein with respect to claim 25. Claim 25 as amended includes a capacitive element in series with the transistor switch to reduce the capacitance contributed by the transistor switch not disclosed in McClure.

With respect to claim 26, the Examiner contends that McClure teaches an ESD protected integrated circuit input comprising an integrated circuit input [Fig. 2, Vcc, 102]; a diode string [Fig. 2, 100] coupled to the integrated circuit input; a transistor switch [Fig. 2, 03, 106] having its gate coupled to the diode string, the transistor switch coupling the integrated circuit input to ground in parallel to the diode string; and a reverse diode [Fig. 2, 116] coupling ground to the integrated circuit input as disclosed in Col. 3, lines 19-25 and lines 44-48.

The remarks made with respect to claim 1 are reincorporated herein with respect to claim 26. Claim 26 as amended includes a capacitive element in series with the

transistor switch to reduce the capacitance contributed by the transistor switch not disclosed in McClure.

Claim Rejections - 35 *USC* § *103*

2. Claims 4, 5, 16, 17, 22 and 29 were rejected as being obvious over McClure, Patent No. 5,774,318, in view of Weiss, Patent No. 6,600,356.

The Examiner cited McClure as teaching an ESD protection circuit coupled to ground, but admitted that McClure does not disclose that the ESD protection circuit further comprises a capacitive element in series with the switching transistor to reduce the capacitance contributed by the switching transistor. The Examiner cited Weiss as teaching an ESD protection circuit that comprises a diode string [Fig. 5, 10] and a switching transistor [Fig. 5, Q1]. The Examiner contended that Weiss further teaches a capacitive element [Fig. 4, D1] in series with the switching transistor [Fig. 4, Q1] to reduce the capacitance contributed by the switching transistor as disclosed in Col. 3, lines 12-30. The Examiner asserted that both teachings are related by being electrostatic discharge protection circuits, so that it would have been obvious to combine the teachings of Weiss, which teaches a capacitive element in series with a switching transistor, with the ESD protection circuit of McClure for the benefit of reducing the susceptibility to power supply transients.

Similar to the McClure, the Weiss is also for protection of positive and negative voltage power supply terminals as stated in col. 1, line 14 - 18. Once again the claimed circuit is for protection of input/output signal path of a RF integrated circuit, as well as the voltage power supply terminals. Because the claimed circuit is used at input/output

signal paths, a diode 24 is connected in series with the switch, so that the loading capacitance is reduced to minimize input/output signal distortion. For voltage power supply terminal protection as used in McClure's circuit and Weiss's circuit, loading capacitance is not an issue since there is no input/output signal involved.

In Weiss's circuit, the two series connected diodes [Fig. 4, D1] are in series with the switching transistor [Fig. 4, Q1], which has its base left floating (unconnected). This circuit configuration is distinctly different from our transistor switch. In Weiss's circuit, the two diodes are used for the purpose of increasing the margin between the normal power supply operating voltage and BVceo , thereby reducing the susceptibility to power supply transients at power supply terminal, as stated in col. 3 line 21-30, and **not** for loading capacitance reduction at signal path as used in the claimed circuit. It further stated in Weiss's claim that the diodes also increase the voltage across the network during avalanche, ensuring that the circuit will not remain conducting when the positive power supply node V+ returns to its normal range. Weiss does not state that the diode is used as a capacitive element and that the diode in series with a switch can be used for loading capacitance reduction as in the claims here. Weiss has no teaching, no motivation nor suggestion that a diode can be used as a capacitance element and that a diode in series with a switch can be used for loading capacitance reduction. The function of capacitance reduction is not inherent in Fig. 4, because the circuit appears on power supply terminals and the capacitance of the single transistor Q1 in Fig. 4 of Weiss is not mentioned since it is not relevance in the operation of the Fig. 4 circuit. No signal distortion reduction from capacitance reduction occurs, because the power supply terminals do not involve signal.

With respect to claim 5, the Examiner contends that Weiss teaches that the switching transistor comprises a single bipolar transistor [Fig. 4, Q1] and the capacitive element comprises a diode [Fig. 4, D1], but does not disclose that the switching transistor comprises a Darlington pair. McClure teaches that a Darlington pair [Fig. 3, Q4, Q5, 106] is preferred over a single transistor [Fig. 2, Q3, 106, Col. 5, lines 55-65]. Therefore, the Examiner concludes that it would have been obvious to replace the switching transistor [Fig. 4, D1] taught by Weiss with the switching transistor [Fig. 3, Q4, Q5, 106] to have a Darlington pair and a diode in series, because the Darlington pair offers a higher gain and thus a faster turn-on time, as well as a higher collector impedance which results in a lower leakage current.

It is not true that the higher collector impedance of Darlington pair results in a lower leakage current as stated by Weiss. The Darlington pair is a switch and the leakage current does not depend on the collector impedance. In the claimed circuit, the added benefit of using a Darlington pair is that the loading capacitance is smaller with a Darlington pair because the size of the diode string 14 can be reduced due to smaller trigger current. A Darlington pair needs smaller trigger current than a single transistor. The Examiner is ignoring the other claimed elements of the circuit, each of which factor in the capacitive load and how it might be reduced. Certainly in the case of Weiss' Fig. 4 there is no diode string similar in any manner to diode string 14 and therefore there is no perceived advantage, motivation, suggestion nor teaching to combine a diode capacitive-reduced Darlington pair with a diode string for use with input/output signal terminals on RF chips.

Claim 17 further defines claim 12 and is allowable therewith for the reasons set forth in connection with claim 5, which are reincorporated herein.

The Examiner rejects claim 22, as being the polar opposite of claim 21, and is an art recognized equivalent configuration to claim 21. However, claim 21 is not disclosed in the cited art in the context of the claim. There being no valid rejection of claim 21, there is similarly no valid rejection of claim 22.

3. Claims 6 and 15 were rejected as being obvious over McClure et al., Patent No. 5,774,318, in view of Ring, Patent No. 3,755,751.

In regard to claim 6 the Examiner cited McClure as teaching an ESD protection circuit coupled to ground but admitted that McClure does not disclose that the ESD circuit further comprises a series diode and a series resistor combined in any order and coupled between the gate of the transistor switch and the diode string on one hand and ground on the other hand.

Ring was cited as teaching a protection circuit for limiting the temperature of an amplifier circuit. The Examiner characterized the protection circuit as comprising a series diode [Fig. 1, 68] and a series resistor [Fig. 1, 70] in any order and coupled between the gate of the transistor switch [Fig. 1, 118]. The Examiner concluded that it would have been obvious to combine the teachings of Ring, which teaches a series diode and a series resistor, with the ESD protection circuit of McClure because the resistor connected to ground keeps triggering the switching transistor off under normal working conditions and also influences the duration of switch-off time of the switching transistor during an ESD event and the use of diode insures that a stray current will now

flow from the ground into the base of the switching transistor. The Examiner contended that the combination of the series diode [Ring, Fig. 1, 68] and series resistor [Ring, Fig. 1, 70] and the diode string [McClure, Fig. 1, 100] and ground [McClure, Fig. 1, GND] was somehow suggested.

Ring's circuit is not an ESD protection circuit. It is a high voltage amplifier circuit with temperature responsive shutdown. The diode and resistor used are for temperature tracking purpose for the bipolar transistor, since the diode and the transistor have the same temperature coefficient. Ring does not motivate, teach or suggest the claimed combination of claim 6, since Ring's circuit element are used for temperature tracking and are not related to any use in an ESD protection circuit.

In the claimed circuit, in order to properly trigger the Darlington pair switch, a resistor/diode pair (20, 22) is needed (claim 6). This resistor /diode pair reduces the leakage current at low to higher RF signal power. If a single resistor 112 is used as in McClure's Fig. 2, large leakage current result that significantly degrade linearity, RF signal power, power consumption, and DC-RF efficiency.

With respect to claim 15, the Examiner contends that McClure teaches that triggering the Darlington pair [Fig. 3, 106] comprises coupling the first type of ESD event through the diode string [Fig. 3, 100] to the gate of the Darlington pair. The Examiner further contends that Ring teaches that triggering the transistor switch comprises coupling the first type of ESD event through the diode string [Fig. 1, 66] to a series diode [Fig. 1, 68] and resistor [Fig. 1, 70] to ground to prevent ESD protection circuit from turning on during low to moderate RF power operation, therefore minimizing leaking current and improving linearity.

The Applicants respectfully disagree with the characterization given to Ring. Ring teaches nothing in regard to triggering a transistor switch by coupling a first type of ESD event through the diode string [Fig. 1, 66] to a series diode [Fig. 1, 68] and resistor [Fig. 1, 70] to ground to prevent ESD protection circuit from turning on during low to moderate RF power operation, therefore minimizing leaking current and improving linearity. There is no mention of an ESD event in Ring. Diode 66 is not a string. The purpose of diode 68 and resistor 70 is for temperature tracking and has nothing whatsoever to do with preventing an ESD protection circuit from turning on during low to moderate RF power operation, to therefore minimize leaking current and improve linearity. Any such characterization of Ring is a severe misreading and mischaracterization of the teachings in Ring.

4. Claims 8 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over McClure et al., Patent No. 5,774,318, in view of Brennan et al., Publication No. US2002/0130392.

Claims 8 and 23 depend on claim 1 and are allowable therewith and for such further limitations are set forth therein.

5. Claims 9 and 10 were rejected as being obvious over McClure et al., Patent No. 5,774,318, in view of Johnson, Patent No. 6,624,999.

The Examiner contends that McClure teaches an ESD protection circuit coupled to ground, but admits that McClure does not disclose that the ESD protection-circuit is coupled to an RF integrated circuit. Johnson is cited as teaching an ESD protection

circuit [Fig. 1, 35-1, 35-2], which is coupled to an RF integrated circuit [Fig. 1, 20, Col. 1, lines 54-55, lines 62-64]. The Examiner concludes that it would have been obvious to combine the teachings of Johnson, which teaches an ESD protection circuit coupled to an RF integrated circuit, with the ESD protection circuit of McClure for the benefit of protecting an integrated circuit operating at a high frequency.

Johnson (Fig. 1) uses off-chip or external inductors 70, 75 as a protection circuit in an RFIC, but has no resemblance to the claimed integrated ESD circuit at claim 9. Again, McClure is directed for protection of voltage power supply terminals as stated in col. 1, line 6-8. The claimed circuit differs in two important respects. The claimed integrated ESD circuit is monolithically integrated with RF integrated circuits (RFIC), and is also provided for protection of input/output signal paths of a RF integrated circuit (as well as the voltage power supply terminals). It does not follow from Johnson's teaching of external protection device and McClure's teaching of circuit for protection of positive and negative voltage power supply terminals that the claimed circuit can be monolithically fabricated with any RF integrated circuits onto the same chip.

6. Claims 11 and 18 - 20 were rejected as being obvious over McClure et al., Patent No. 5,774,318, in view of Weiss, Patent No. 6,600,356 as applied to claims 1-5 above, and further in view of Ring, Patent No. 3,755,751.

With respect to claim 11, the Examiner contends that McClure teaches an ESD protection circuit coupled to ground comprises an input [Fig. 3, Vcc, 102]; a diode string [Fig. 3, 100] coupled to the input; a Darlington pair [Fig. 3, 106] having its gate coupled to the diode string, the Darlington pair coupling the input to ground in parallel to the

diode string; and a reverse diode [Fig. 3, 116] coupling ground to the input where the diode string is forward biased on the application of positive ESD events at the input and the reverse diode is forward biased on the application of negative ESD events at the input [Col. 3, lines 19-25, 44-48, Col. 5, lines 7-16, Col. 6, lines 18-21].

However, the Examiner admits that McClure does not disclose a series diode, a series resistor and a diode in series with the Darlington pair to reduce the capacitance contributed by the Darlington pair. With respect to the limitation of a diode in series with a Darlington pair, the Examiner contends that Weiss teaches an ESD protection circuit that comprises coupling the input [Fig. 5, V+] to ground [Fig. 5, GND] during ESD protection by means of a capacitive element [Fig. 4, D1] in series with the transistor switch [Fig. 4, Fig. 5, Q1] to reduce the capacitance contributed from the transistor switch [Col. 3, lines 12-30], but the Examiner admits that Weiss does not disclose a diode in series with a Darlington pair to reduce the capacitance contributed from the Darlington pair. The Examiner contends that McClure teaches that a Darlington pair [Fig. 3, Q4, Q5, 106] is preferred over a single transistor [Fig. 2, Q3, 106, Col. 5, lines 55-65]. The Examiner concludes that it would have been obvious to replace the switching transistor [Fig. 4, Q1] taught by Weiss with the switching transistor [Fig. 3, Q4, Q5, 106] to have a Darlington pair and a diode in series to reduce the capacitance contributed by the Darlington pair, because the Darlington pair offers a higher gain and thus a faster turn-on time, as well as a higher collector impedance which results in a lower leakage current. The Examiner further cites Ring as teaching a series diode [Fig. 1, 68] and a series resistor [Fig. 1, 70], where the series diode and the series resistor are coupled in series with each other and their combination is coupled between the gate

of the Darlington pair (taught by McClure). The Examiner concludes that it would have been obvious to combine the teachings of Ring, which teaches a series diode and a series resistor, with the ESD protection circuit of McClure modified by Weiss, because the resistor connected to ground keeps triggering the switching transistor off under normal working conditions and also influences the duration of switch-off time of the switching transistor during an ESD event and the use of diode ensures that a stray current will not flow from the ground into the base of the switching transistor. In this configuration, the Examiner contends that the series diode [Ring, Fig. 1,68] and series resistor [Ring, Fig. 1, 70] and the diode string [McClure, Fig. 1, 100] would be on one hand and ground [McClure, Fig. 1, GND] on the other hand.

The foregoing rejection is a combination of separate rejections, each of which have been cited and discussed above. The above remarks in pertinent part are herein reincorporated in regard to claim 11.

By way of reference to the foregoing remarks, McClure's circuit is **not** for ESD protection of input/output signal terminals, but for protection of positive and negative voltage power supply terminals as stated in col. 1, line 6-8. Weiss's circuit is **not** for ESD protection of input/output signal terminals, but is also for protection of positive and negative voltage power supply terminals as stated in col. 1, line 14-18. Ring's circuit is **not** an ESD protection circuit. It is a high voltage amplifier circuit with temperature responsive shutdown. The diode and resistor is **not** used for biasing a Darlington pair, but is used are for temperature tracking purpose for the bipolar transistor, since they have the same temperature coefficient.

The circuit claimed at claim 11 is a circuit for protection of input/output signal paths integrated with a RF integrated circuit. This is a completely different application that protection from supply voltage spikes. ESD protection at signal path is more difficult and different than that at the voltage power supply terminal. Unlike protection of a voltage power supply terminal, extra loading capacitance at signal path can distort signal at an input/output signal terminal, which is not acceptable. Furthermore, extra leakage current during low to moderate RF power operation can degrade the RF signal linearity at an input/output signal terminal, which is not acceptable.

Because the claimed circuit is used at input/output signal paths, a diode 24 is connected in series with the switch 16, so that the switch 16's loading capacitance is reduced to minimize input/output signal distortion. For voltage power supply terminal protection as used in McClure's and Weiss's circuit, loading capacitance is not an issue since there is no input/output signal involved.

In the claimed circuit, in order to properly trigger the Darlington pair switch, a resistor/diode pair (20, 22) is also needed. This resistor /diode pair reduced the leakage current at low to higher RF signal power. If a single resistor is used as in McClure's and Weiss's circuit, large leakage current would result that would affect linearity, RF signal power, and DC power consumption, and DC-RF efficiency. In Ring's circuit, the resistor/diode pair is used for temperature tracking, which is unrelated and is a completely different application.

The circuitry claimed in claim 11 and claims 6, 15, 18 includes voltage overload protection for RF power amplifiers for conditions of (1) output impedance mismatch, (2) RF overdrive, and (3) modulated input signal. The collector output of an RF power

amplifier is usually connected with a RF inductor (often called RF choke) and an output impedance matching network. The other side of the output impedance matching network is terminated with a termination, such as an antenna. The voltage at the transistor collector output is described by $Vo = Vs + L\frac{di}{dt}$. As a result, this voltage can be higher than the supply voltage. Furthermore, how high this voltage would be also depends on the impedance of the output impedance matching network.

In an output impedance mismatch condition, such as the cases of loose or obstructed antenna, the reflected signal reflects back to the transistor and produces a large voltage waveform so severe that the transistor junctions can be damaged. Furthermore, the power amplifier, due to the requirement of delivering high output power with high efficiency, often operates at overdrive condition, in which the transistor input voltage is so high that it switches on and off the collector current. During overdrive, the transistor can be modeled as a switch and inductor in parallel with a capacitor as shown below in Fig. 1.

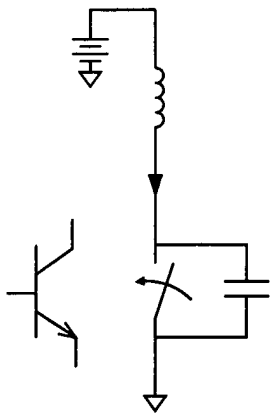


Fig. 1 Transistor modeled as a switch for RF overdrive

When the switch is shorted, the current through the inductor is at maximum. As soon as the switch is opened, since the inductor current cannot be zero instantaneously, the inductor current flows to the transistor capacitance and the output impedance network. Because of an enormous inductor current, the transient voltage at the collector output can be very high. This excessive voltage overload can lead to device failure and degradation in reliability if it is higher than the breakdown voltages.

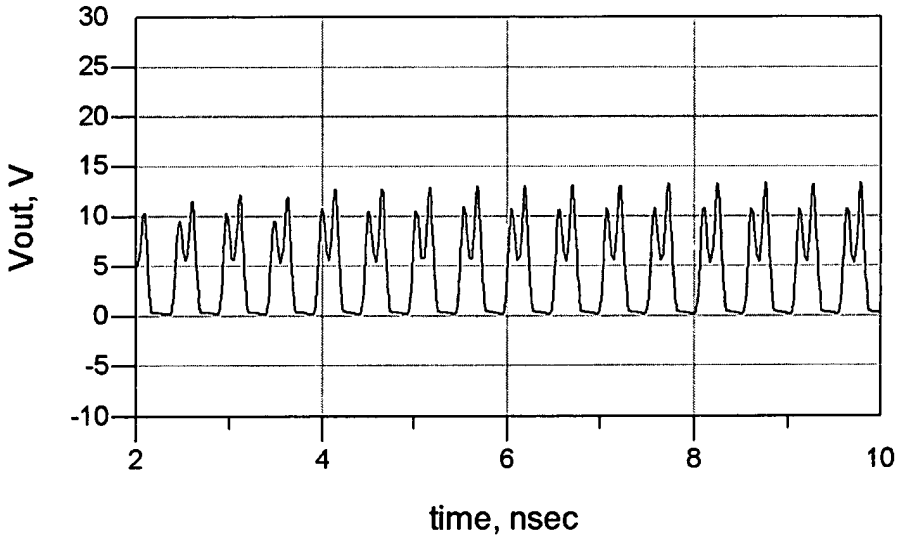
Even when the output termination impedance is 50 ohm, the transient collector output voltage waveform during RF overdrive can be larger than the breakdown voltage as shown in Fig. 2a below. Since the excess voltage as shown is positive, the C-E and C-B junction are vulnerable.

Output impedance mismatch and modulated input signal combining with overdrive can make the voltage overload more severe. For open termination combining with RF overdrive, such as the case when antenna is not connected, the output voltage is the most severe as shown in Fig. 2b. The transient output voltage is so large that it even goes negative in which case the E-B junction is also vulnerable.

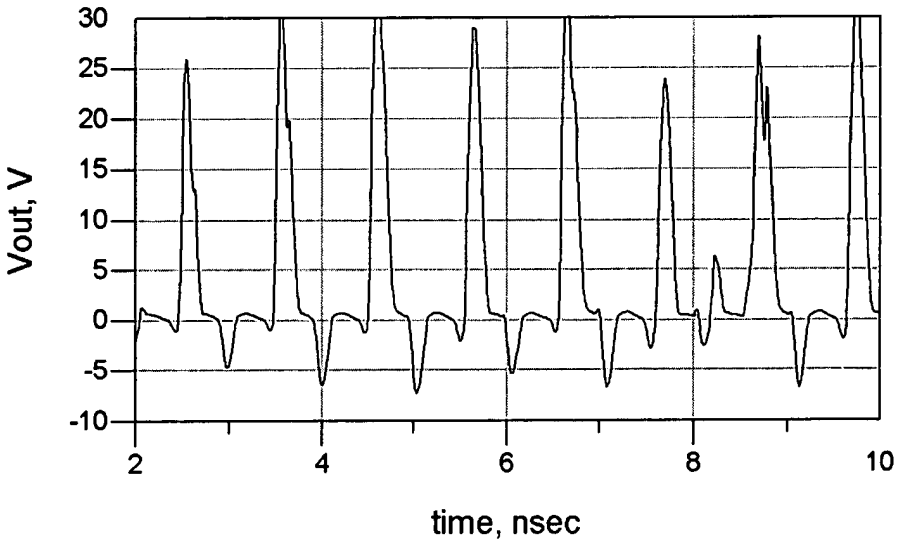
For the shorted termination combining with RF overdrive, although the voltage overload is not as severe, Fig. 2c, as the open termination, it is still more severe than a 50 ohm case.

Modulation of input signal can add additional transient output voltage. With just a simple AM modulation with a pulse train combining with RF overdrive, the voltage overload does get worst as shown in Fig. 2d. For a multiple stage amplifier, the voltage overload at the output stage can be even worse if the driver stages are overdriven,

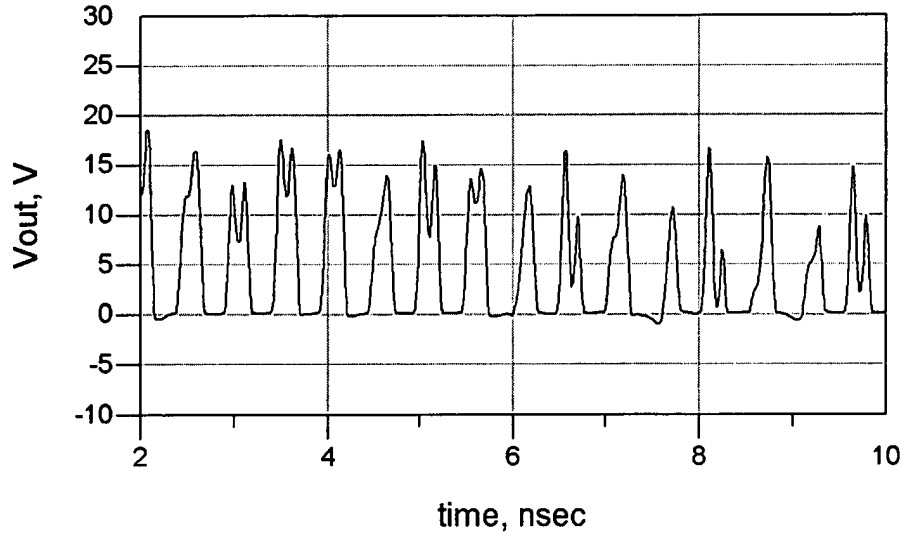
since the voltage spikes of the driver stages would be amplified by the output stages. Usually, the transistor failures due to voltage overload occurs at the output stage, but they can also occur at the driver stages.



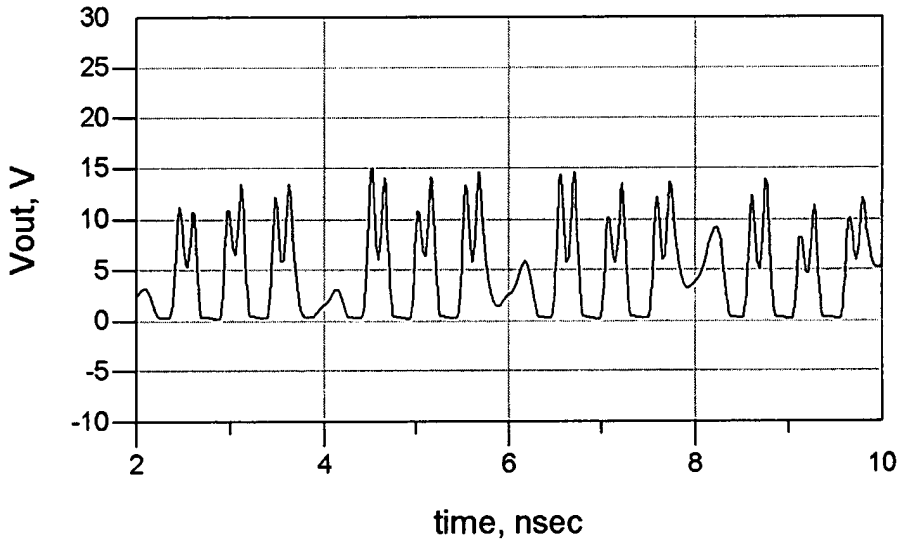
(a)



(b)



(c)



(d)

Fig. 2 Simulated voltage waveform at the collector output for a WCDMA power amplifier during RF overdrive when output termination is (a) 50 ohm, (b) open, (c) short, and (d) 50 ohm and the input signal is AM modulated with pulses.

The function of the voltage overload protection circuit of claim 11 is to clamp the excess voltage to a safe level and bypass the excess current away from the transistor.

This voltage clamp design should take into consideration the voltage swing of the signal so the operation of the power amplifier is not interfered. The voltage overload protection circuit must have low loading capacitance, so the RF performance is not affected.

The applications of the earlier invented ESD protection circuits are extended by the invention to include their use as the voltage overload protection circuit for output impedance mismatch, RF overdrive, and modulated input signal conditions. They will be reviewed in the following with two different circuits. Their schematics are shown in Fig. 3 and Fig. 4 below respectively. For drawing Fig. 3 below, the positive threshold voltage trigger is comprised of a diode string in series with a single resistor; they are used to trigger a bipolar transistor switch in series with a diode. For Fig. 4 below, the positive threshold voltage trigger consists of a diode string in series with a single diode and a single resistor; they are used to trigger a Darlington pair transistor switch in series with a diode. For the same circuit providing both ESD and voltage overload protection, the number of diodes can be carefully selected. The reverse diode in both drawings can be used for clamping excess negative voltage.

Fig. 5 below shows the transistor output waveform with the voltage overload protection circuit clamping the excess voltage. The turn on time of the voltage overload protection circuit is very fast, less than 20psec, as shown in Fig. 6 below. To protect the SiGe HBT power amplifiers, the same protection circuit topology as shown in Figs. 3 & 4 can be implemented by the SiGe HBTs. Since SiGe HBT has lower breakdown than GaAs HBT, this voltage overload protection circuit is very important for improving reliability of SiGe HBT power amplifiers.

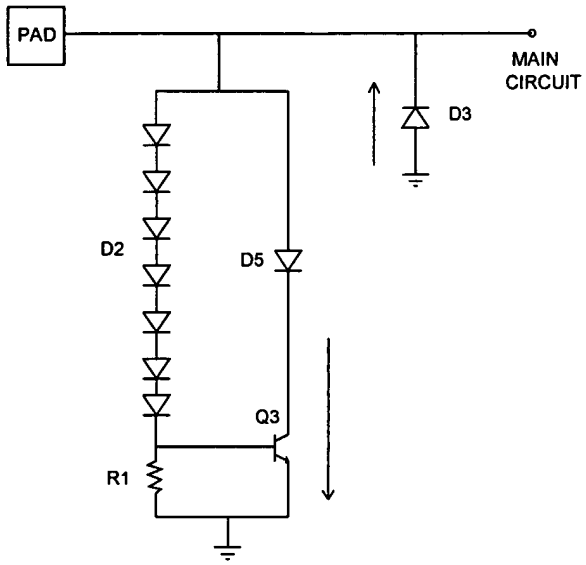


Fig. 3 On-chip voltage ESD/overload protection circuit using single bipolar transistor, drawing A

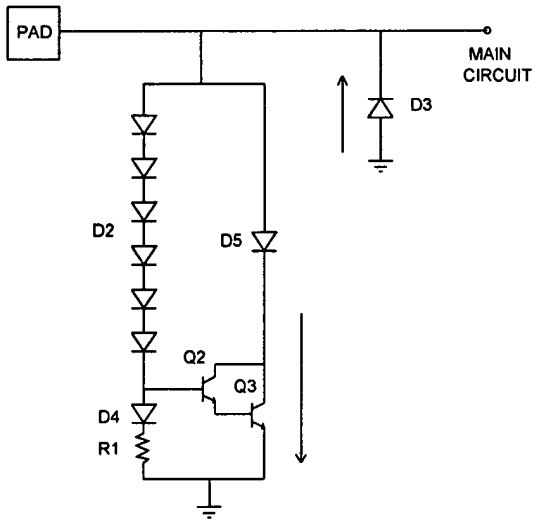


Fig. 4 On-chip ESD/voltage overload protection circuit using Darlington pair, drawing B

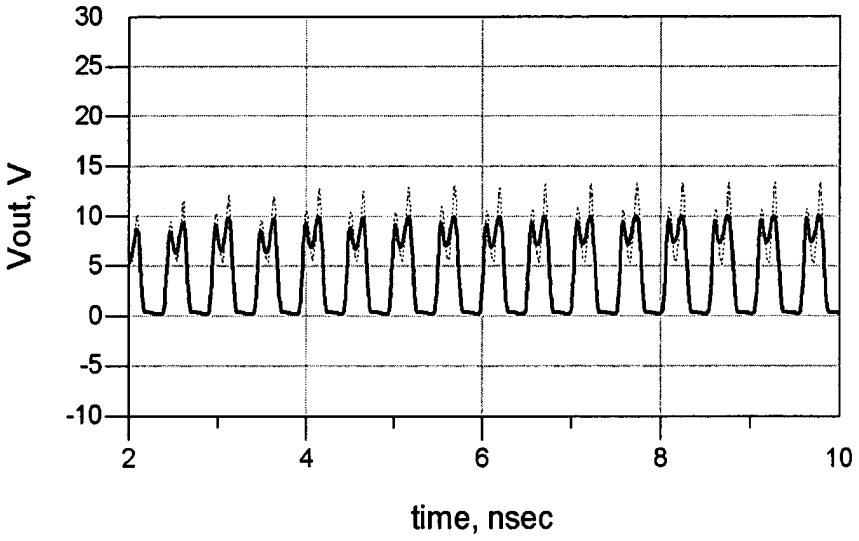


Fig. 5 Simulated collector output voltage waveform during RF overdrive when output termination impedance is 50 ohm and the collector output is connected (a) with (solid) and (b) without (dot) voltage overload protection circuit.

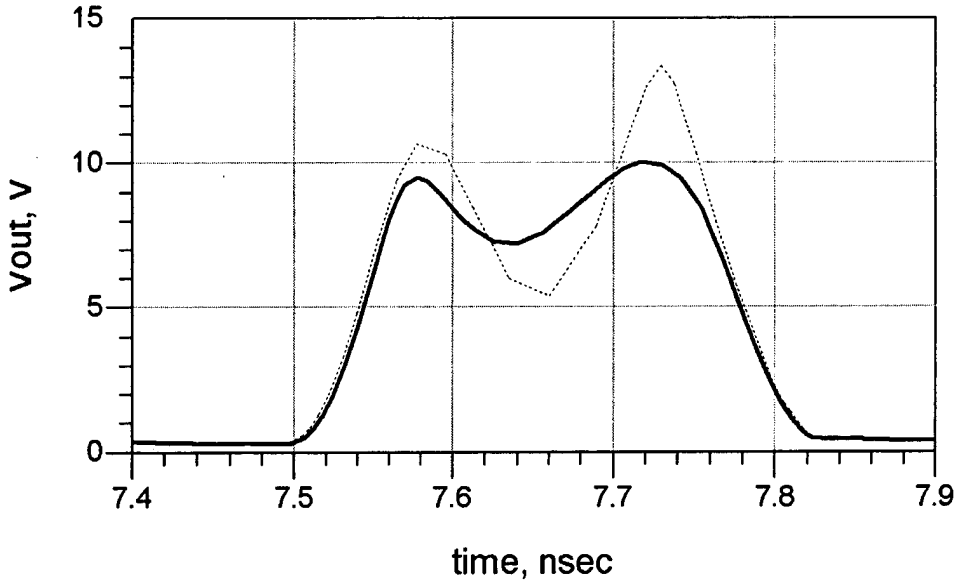


Fig. 6 Close up of Fig. 5.

With respect to claim 18, the Examiner contends that McClure teaches a method for providing ESD protection comprising sinking a first type of ESD event to ground [Fig.

3, 104] from an input through a diode string [Fig. 3, 100] coupled to the input by triggering a Darlington pair [Fig. 3, 106], the Darlington pair coupling the input to ground in parallel to the diode string; and a second type of ESD event through a reverse diode [Fig. 3, 116] coupling ground to the input. However, McClure does not disclose a series diode, a series resistor, and a diode in series with the Darlington pair to reduce the capacitance contributed to the diode string from the Darlington pair. The Examiner contends that Weiss teaches coupling the input [Fig. 4, V+] to ground [Fig. 4, GND] during the ESD protection by means of a diode [Fig. 4, 01] in series with the Darlington pair (or a switching transistor) to reduce the capacitance contributed to the diode string from the Darlington pair. The Examiner contends that Ring teaches coupling the first type of ESD event through the diode string [Fig. 1, 66] to a series diode [Fig. 1, 68] and resistor [Fig. 1, 70] to ground [Fig. 1, Vcc] to prevent the ESD protection circuit from turning on during low to moderate RF power operation, therefore minimizing leaking current and improving linearity.

The foregoing rejection is a combination of separate rejections, each of which have been cited and discussed above in connection with claim 11. The above remarks in pertinent part are herein reincorporated in regard to claim 18. Further, the Applicants disagree with the characterization give to Ring as stated above in connection with claim 15.

With respect to claim 19, the Examiner contends that McClure teaches that the first type of ESD event is a positive voltage surge applied to the input [Fig. 2, Vcc, 102, Col. 3, lines 19-25]. and the second type of ESD event is a negative voltage surge applied to the input[Col. 5, lines 7-16, Col. 6, lines 18-21].

Claim 19 depends on claim 18 and is allowable therewith and further serves to define the steps of claim 18.

The Examiner contends that with respect to claim 20, the limitation is the polar opposite of claim 19, and is an art recognized equivalent configuration.

The Examiner rejects claim 20, as being the polar opposite of claim 19, and is an art recognized equivalent configuration to claim 19. However, claim 19 is not disclosed in the cited art in the context of the claim. There being no valid rejection of claim 19, there is similarly no valid rejection of claim 20.

8. Claims 27 and 30 were rejected as being obvious over McClure, Patent No. 5,774,318, in view of Voldman, Patent No. 5,945,713.

The Examiner contended that McClure teaches an ESD protection circuit coupled to ground, but admitted that McClure does not disclose that chip-layout size of the transistor switch and diode string when used in combination is smaller than the chip-layout size of a diode string when used alone.

The Examiner contended that Voldman teaches an electrostatic discharge protection circuit and teaches that the transistor switch and diode string each have a chip-layout size and where the chip-layout size of the transistor switch and diode string when used in combination is smaller than the chip-layout size of a diode string when used alone, which used-alone diode string provides substantially the same ESD protection as the transistor switch and diode string in combination as characterized by the maximum clamping voltage of the ESD protection circuit [Col. 3, lines 44-50]. The Examiner contended that it would have been obvious to combine the teachings of

Voldman with the ESD protection circuit of McClure in order to avoid electrical overstress and prevent undesirable current leakage paths that create system-level power loss.

In Voldman (col. 3, line 44-50), transistor scaling is mentioned which can reduce transistor size, but **not** the circuit layout size as claimed. The characterization given to Voldman above seriously distorts the teaching of the reference in regard to chip-layout size of the ESD circuit combinations. In the claimed circuit, because the use of diode string and transistors are the preferred embodiment, a smaller trigger current is sufficient to turn on the ESD protection device. Because of the smaller trigger current needed in the ESD protection circuit, a smaller size diode string can be used so that the layout of the ESD protection circuit and its equivalent loading capacitance are consequently reduced. There is no teaching in any of the cited references to this effect.

The Examiner contends that with respect to claim 30, it would have been obvious to place the ESD circuit where there is a space to accommodate the circuit and its required electrical connections.

Claim 30 depends on claim 27 and is allowable therewith, and serves to further define chip-layout sizes and the advantages flowing from the claimed limitations.

Applicant respectfully requests advancement of the claims to allowance.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on May 3, 2006 by

Signature

5/3/2006

May 3 2006

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APPENDIX